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FLASH ARRAY IMPLEMENTATION WITH LOCAL AND GLOBAL BIT LINES

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Cross-reference to related application

[0001] This is a divisional application of U.S. Patent Application Serial No. 10/017,664, titled FLASH ARRAY IMPLEMENTATION WITH LOCAL AND GLOBAL BIT, filed December 12, 2001 (~~pending~~), which application is assigned to the assignee of the present invention and the entire contents of which are incorporated herein by reference.

now US patent No. 6,795,326

Technical Field of the Invention

[0002] The present invention relates generally to non-volatile memory devices and in particular the present invention relates to global and local bit line designs in synchronous non-volatile flash memory.

Background of the Invention

[0003] Memory devices are typically provided as internal storage areas for computers. The term "memory" identifies data storage that comes in the form of integrated circuit chips. There are several different types of memory, including RAM (random-access memory). RAM is typically used as main memory in a computer environment. Most RAM is volatile, which means that it requires a steady flow of electricity to maintain its contents. As soon as the power is turned off, whatever data was in RAM is lost.

[0004] Computers can contain a small amount of read-only memory (ROM) that holds instructions for starting up the computer. An EEPROM (electrically erasable programmable read-only memory) is a special type of non-volatile ROM that can be erased by exposing it to an electrical charge. Like other types of ROM, EEPROM is traditionally not as fast as RAM. EEPROM comprise a large number of memory cells having electrically isolated gates (floating gates). Data is stored in the memory cells in